



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Whitman et al.

Serial No.: 09/542,783

Filed: April 4, 2000

For: SPIN COATING FOR MAXIMUM
FILL CHARACTERISTIC YIELDING A
PLANARIZED THIN FILM SURFACE

Confirmation No.: 6870

Examiner: B. Kebede

Group Art Unit: 2823

Attorney Docket No.: 2269-4294US
(98-1208.00/US)

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In compliance with the duty to disclose information material to patentability pursuant to 37 C.F.R. § 1.56, it is respectfully requested that this Supplemental Information Disclosure Statement be entered and the documents listed on attached Form PTO-1449 or PTO/SB/08 be considered by the Examiner and made of record. Copies of the listed documents are enclosed pursuant to 37 C.F.R. § 1.98(a).

In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an

admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

<u>U.S. Patent No.</u>	<u>Publication Date</u>	<u>Patentee</u>
US - 6,251,487	June 26, 2001	Yonaha

Other Documents

WOLF, STANLEY AND TAUBER, RICHARD, Silicon Processing for the VLSI Era, Volume 1: Process Technology, pp. 429-434, Lattice Press, Sunset Beach , California 1986

Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

This Supplemental Information Disclosure Statement is believed to be filed before the mailing date of the first Office Action on the merits subsequent to the filing of an RCE in the above-identified application.

Respectfully submitted,

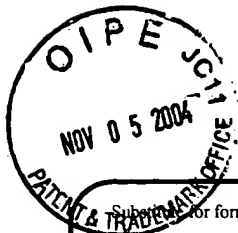


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Date: November 5, 2004
BGP/nj:rh

Enclosures: Form PTO-1449 or PTO/SB/08
Copy of documents cited

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PTO/SB/08B(10-03)

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Sheet

2

of

2

Complete if Known

Application Number	09/542,783
Filing Date	April 4, 2000
First Named Inventor	Whitman et al.
Group Art Unit	2823
Examiner Name	B. Kebede
Attorney Docket Number	2269-4294US (98-1208 00/US)

NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		WOLF, STANLEY AND TAUBER, RICHARD, Silicon Processing for the VLSI Era, Volume 1: Process Technology, pp. 429-434, Lattice Press, Sunset Beach, California 1986	

Examiner
Signature

Date

Considered

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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